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REMARKS

Reconsideration of the application is requested.

Claims 1-25 are in the application. Claims 1-25 were rejected in the above-identified Office Action. Claims 1 and 15 have been amended.

Applicants acknowledge the Examiner's confirmation of receipt of applicants' certified copy of the priority document in item 3 on page 2 for the German Patent Application 198 43 663.7, filed September 23, 1998 supporting the claim for priority under 35 U.S.C. § 119.

Regarding item 4 on page 2, as noted in the information disclosure statement filed September 8, 2003, for which the Examiner acknowledged receipt in item 2 on page 2 of the above-identified Office Action, documents J, K, and L on applicants' Form PTO-1449 directly correspond to U.S. Patent No. 5,784,636 to *Rupp*, U.S. Patent No. 5,794,062 to *Baxter*, and U.S. Patent No. 6,061,367 to *Siemers* listed on the previously identified form PTO-1449 as documents B, C, and D respectively. As such, the applicants respectfully submit that since the Examiner has already considered documents B, C, and D the corresponding documents J, K, and L have also already been considered by the Examiner and should be

initialed by the Examiner for inclusion with the other references.

In "Specification" item 5 on page 2 of the above-identified Office Action, the Examiner objected to the title as not being sufficiently descriptive. The Examiner's suggested corrections have been considered and an amendment based on the Examiner's suggestions has made.

In "Specification" item 6 on page 2 of the above-identified Office Action, the Examiner objected to the abstract of the disclosure as not being on a separate sheet. The applicant traverses the Examiner's objection as a copy of the Abstract of the Disclosure was previously provided separately. The applicant respectfully requests that the Examiner review the file again to determine whether the Abstract may have been misfiled and included with the declaration. Alternatively, the applicant has included a copy of the originally submitted Abstract of the Disclosure as an appendix to this response. Moreover, applicant has included a request to replace the "missing" abstract with the amended abstract.

In "Specification" item 7 on page 2 of the above-identified Office Action, the Examiner objected to the use of the term ">S<puter" as not having an unknown meaning. Respectfully,

the applicant traverses the Examiner's objection as ">S<puter" is a term that would be known to one of skill in the art. An Internet search conducted on www.Google.com using the term ">S<puter" revealed at least 213 qualifying references (although applicants respectfully note that it does appear that the slang term "'s puter" referring to someone's computer was also frequently included in the search results). Several of the early references in the Internet search were even written by the above-named inventors of the instant application. Moreover and more importantly, the specification provides more than adequate definition of the term. Among other examples in the specification, the following excerpts from the specification of the instant application help illustrate the more than adequate descriptions:

> Configurable hardware blocks can also be used in program-controlled units, and their use in so-called >S<puters is well documented. (Page 2, lines 1-3).

> The aforementioned >S<puter is a program-controlled unit that can process more than one instruction per processor cycle. European published patent application EP 0 825 540 A1 and U.S. Patent No. 6,061,367 describe an exemplary embodiment of one such >S<puter. (page 3, lines 4-8).

> Referring now more specifically to Fig. 3, the >S<puter includes a predecode unit (1), an instruction buffer (2), a decode, rename & load unit (3), an s-unit (4), a data cache (5), and a memory interface (6). The s-unit (4) comprises a programmable structure buffer (41), a functional unit with programmable structure (42), an integer/address instruction buffer (43), and an integer register file (44). (page 3, lines 19-25).

In "Specification" item 8 on page 3 of the above-identified Office Action, the Examiner requests applicants' assistance in correcting any errors in the specification, especially those due to unclear terms and translation errors, which upon discovery of such terms or errors the applicants will gladly provide. Accordingly, a typographical error found on page 6 is corrected in this amendment.

In "Specification" item 9 on page 3 of the above-identified Office Action, the Examiner objected to the listing of the references on page 27 and 28 of the specification, as being unclear whether the references were intended to be incorporated by reference or used as information disclosure statement material.

Applicants respectfully note that the references were provided to "provide further details about hyperblocks, other instruction blocks, and related topics" and as such applicants believe the references are properly presented as an aid to those not of skill in the art to better understand the invention. It is thus the applicants' belief that those of skill in the art would know hyperblocks, instruction blocks, and other related topics. Thus, the references listed on pages 27 and 28 were not intended to be incorporated by reference, nor are the references considered

"essential" or "material" to warrant mandatory inclusion in an information disclosure statement. As indicated in MPEP § 2001:

> Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section.

In the instant case, the items taught by the references are not considered material to the patentability of the claims. As MPEP § 2001.05 clarifies:

> If information is not material, there is no duty to disclose the information to the Office.

In spite of this belief, undersigned counsel has requested that the applicants review the references and determine whether the materials could be considered "essential" or "material" to the patent application. If the references are determined to be material to patentability as previously discussed, undersigned counsel will file an information disclosure statement upon receipt of copies of the references.

In "Claim Objections" item 10 on page 3 of the above-identified Office Action, the Examiner objected to claim 15 as being unclear whether "a multiplexer series-connected" is intended to mean "a multiplexer connected in series" or "a

multiplexer series" connected to the comparison units. The Examiner's suggested corrections to claim 15 have been made.

In "Claim Objections" item 11 on page 4 of the above-identified Office Action, the Examiner objected to claims 23 and 24 as depending on claim 21 but being separated by claim 22 that does not depend from claim 21. However, as noted in MPEP 608.01(n):

> During prosecution, the order of claims may change and be in conflict with the requirement that dependent claims refer to a preceding claim. Accordingly, the numbering of dependent claims and the numbers of preceding claims referred to in dependent claims should be carefully checked when claims are renumbered upon allowance.

In the instant application, the claims in question (previously written as multiple dependent claims) and their numbering order are based on the original German and PCT claims. In the process of prosecution for the US application, the multiple dependencies previously found in the international version of claims 23 and 24 were eliminated and both claims currently only depend on claim 21. The resulting numbering of the claims relative to dependencies also changed. Upon allowance of the claims, applicants agree that, in accordance with MPEP 608.01(n), "claims should be carefully checked when claims are renumbered upon allowance" to properly renumber the claims in question.

In "Claim Objections" item 12 on page 4 of the above-identified Office Action, the Examiner objected to claim 24 as using the term "identification application" which is allegedly not defined in the specification. Applicants note that the specification does discuss the use of universal configurable block or UCB for cryptographic and identification applications on page 11 line 16, page 44 line 3, and page 46 lines 6, 10, and 16. The Examiner is encouraged to review pages 44 to 46 and interpret the claim language in light of this description. Moreover, applicants respectfully traverse the Examiner's position that an identification application is not a term well known in the microprocessor art and more particularly, in the configurable hardware art.

In "Claim Rejections - 35 USC § 112" item 14 on page 4 of the above-identified Office Action, claims 1-25 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner states in item 15 on page 4 that there is insufficient antecedent basis in claim 1 to use "the improvement" and indicates in item 16 on page 5 that "In a configurable hardware block" is also improper. Accordingly, applicants have amended claim 1 in accordance

with the Examiner's suggested corrections so that the scope is more consistent with the specification.

Support for these changes may be found on pages 5, 13, and 19 of the specification of the instant application.

It is accordingly believed that the specification and the claims meet the requirements of 35 U.S.C. § 112, first and second paragraphs. The above-noted changes to the claims are provided solely for clarification or cosmetic reasons. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In "Claim Rejections - 35 USC § 102" item 18 on page 5 of the above-identified Office Action, claims 1-11, 16-22, and 24-25 have been rejected as being fully anticipated by U.S. Patent No. 5,794,062 to *Baxter* (hereinafter **BAXTER**) under 35 U.S.C. § 102(e).

In "Claim Rejections - 35 USC § 103" item 40 on page 12 of the above-identified Office Action, claims 12-14 have been rejected as being obvious over **BAXTER** in view of U.S. Patent No. 5,784,636 to *Rupp* (hereinafter **RUPP**) under 35 U.S.C. § 103(a).

In "Claim Rejections - 35 USC § 103" item 44 on page 14 of the above-identified Office Action, claim 15 has been rejected as being obvious over **BAXTER** in view of **RUPP** and further in view of *Hennessy* (hereinafter **HENNESSY**) under 35 U.S.C. § 103(a).

In "Claim Rejections - 35 USC § 103" item 46 on page 15 of the above-identified Office Action, claim 23 has been rejected as being obvious over **BAXTER** in view of *DeHon* (hereinafter **DEHON**) under 35 U.S.C. § 103(a).

The rejections have been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on pages 13 and 19 of the specification of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a configurable hardware block including:

> **a universal configurable unit** being selectively configured to read data stored in a memory unit, to process the data in at least one of arithmetic and logical processing units, and to write data

representing a result of the processing to the memory unit, the universal configurable unit having **an asynchronous combinational circuit to asynchronously link components** of the universal configurable unit, and the universal configurable unit being capable of **interacting autonomously with external hardware.**

The **BAXTER** reference discloses system for dynamically reconfigurable computing using a processing unit with changeable internal hardware. More specifically, the system in **BAXTER** includes a set of S-machines each having a corresponding T-machine, which are coupled to a General Purpose Interconnect Matrix that is coupled to a set of I/O T-machines, a set of I/O devices, and a master time-base unit. While each S-machine in **BAXTER** is a dynamically reconfigurable computer having a memory and a Dynamically Reconfigurable Processing Unit (DRPU), the **BAXTER** systems are not "asynchronously" linked as recited in claim 1 of the instant application. Nor are the devices in **BAXTER** capable of "**interacting autonomously with external hardware**" as recited in claim 1 of the instant application.

Clearly, **BAXTER** does not show "**a universal configurable unit** ... having **an asynchronous combinational circuit to asynchronously link** components of the universal configurable unit ... and ... **interacting autonomously with external hardware**" as recited in claim 1 of the instant application.

The **RUPP** reference discloses reconfigurable computer architectures for use in signal processing. The reconfigurable processor architecture uses a programmable logic structure called an Adaptive Logic Processor (ALP) that is similar to an extendible field programmable gate array (FPGA). A reconfigurable pipeline instruction control loads instructions into the ALP and coordinates the operations of the ALP.

While **RUPP** does include "an autonomous data transfer signal for controlling execution of an autonomous data transfer **between the adaptive logic processor and another element of the reconfigurable computing component**, wherein the autonomous data transfer is independent of an instruction in the executing set of instructions" as stated in claim 5 of **RUPP**, this "autonomous" data transfer is clearly "between" components of **"the reconfigurable computing component"** and **NOT "with external hardware"** as recited in claim 1 of the instant application. Moreover, the Autonomous Pipeline Segment (APS) type circuits are used primarily for asynchronous interfaces **to external sensors and actuators** not "to asynchronously link components" as recited in claim 1 of the instant application.

Clearly, **RUPP** does not show "**a universal configurable unit** … having **an asynchronous combinational circuit to asynchronously link** components of the universal configurable unit … and … **interacting autonomously with external hardware**" as recited in claim 1 of the instant application.

The disclosed Multiplexor portion of "Computer Organization and Design" (1997) in the **HENNESSY** reference discloses that multiplexors can be created with an arbitrary number of data inputs. Moreover, **HENNESSY** indicates that the number of selector inputs may be based on the overall number of data inputs. Additionally, **HENNESSY** indicates that "no datapath resource can be used more than once per instruction" and as a result a memory "separate from one for data" is necessary for instructions. However, a datapath element may be shared through a multiplexor or data selector to control which instruction class uses the datapath resource.

Clearly, **HENNESSY** does not show "**a universal configurable unit** … having **an asynchronous combinational circuit to asynchronously link** components of the universal configurable unit … and … **interacting autonomously with external hardware**" as recited in claim 1 of the instant application.

The **DEHON** reference discloses coupling processors with reconfigurable logic. **DEHON** indicates that "direct hooks" allow the reconfigurable hardware to "monitor" on-chip signals and datapaths. However, **DEHON** provides no indication that the reconfigurable hardware may be "configured to test an integrated circuit" as recited in claim 23 of the instant application. There is a substantial difference between monitoring and debugging (both reactionary activities) and testing (which is an active process) a system. Accordingly, applicants respectfully traverse the corresponding assertion in the office action that because "monitoring and debugging of a reconfigurable logic system" take place "the system and integrated circuit containing the configurable hardware is tested."

This distinction is more clarified on page 44 in the specification of the instant application, where it states:

> The aforementioned chip tests refer in particular to chip tests conducted using test modules that are packaged in the integrated circuit to be tested, primarily therefore the Memory Build in Self Test (MBIST), Linear Feedback Shift Register (LFSR), Multiple Input Signature Register (MISR), Memory Build in Self Repair (MBISR), analogue BIST (in the case of analogue/digital converters, for example), and On-Chip Monitors (current-measurement monitors for IDDQ, for example), etc.

Specifically, the "specific circuit" that the configurable hardware replaces "to test an integrated circuit" as recited

in claim 23 of the instant application refer to "Build in Self Test" modules.

Clearly, **DEHON** does not show "**a universal configurable unit** ... having **an asynchronous combinational circuit to asynchronously link** components of the universal configurable unit ... and ... **interacting autonomously with external hardware**" as recited in claim 1 of the instant application. Nor does **DEHON** teach or suggest replacing "a specific circuit" with a configurable hardware block "configured to test an integrated circuit" as recited in claim 23 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-25 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a

telephone call so that, if possible, patentable language can be worked out.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $110.00 in accordance with Section 1.17 is enclosed herewith.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099. Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

K. H. Flindt

For Applicants

Kyle H. Flindt
Reg. No. 42,539

July 12, 2004

Lerner and Greenberg, P.A.
P.O. Box 2480
Hollywood, Florida 33022-2480
Tel.: (954) 925-1100
Fax: (954) 925-1101

Abstract of the Disclosure

The configurable hardware block is designed to read data stored in a memory according to its configuration, to process the read-out data arithmetically and/or logically and to write the data representing the result of the processing into the memory. The hardware block is capable of interacting with external hardware, thereby providing a flexible and universally applicable hardware block.